AzureWave Technologies, Inc.

AW-CM276NF

IEEE 802.11a/b/g/n/ac Wireless LAN 2T2R and Bluetooth 5.1 Combo Module (M.2 1216)

Datasheet

Rev. F

0B

(For Standard)

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Features

WiFi

- PCIe M.2 TYPE 1216: 16mm(L) x 12mm(W) x 1.85 mm(H)(Max), 130pins LGA package
- SDIO 3.0 or PCIe support for WLAN
- Sub-meter accuracy WiFi indoor locationing(802.11mc)
- Multiple power saving modes for low power consumption
- IEEE 802.11i for advanced security
- Quality of Service (QoS) support for multimedia applications
- Support China WAPI
- Lead-free design

Bluetooth

- UART interfaces support for Bluetooth
- High speed UART,PCM interfaces
- Audio Codec interface support
- Bluetooth 5.1 compliant with Bluetooth 2.1 + Enhanced Data Rate (EDR)

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Revision History

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Version	Revision Date	DCN NO.	Description	Initials	Approved
A	2019/10/23	DCN016172	● Initial Version(new format)	Renton Tao	NC Chen
B	2020/02/05	DCN016708	● Add configuration table for Host interface	Renton Tao	NC Chen
C	2020/06/16	DCN017530	● Remove watermark ● Correct typo	Renton Tao	NC Chen
D	2020/10/26	DCN018877	● Add BT SDIO support for host I/O	Renton Tao	NC Chen
E	2020/11/18	DCN019231	● Add WPA3 supported	Renton Tao	NC Chen
F	2021/04/08	DCN021289	● Add pin numbers description ● Change to new format ● Update chipset vendor to NXP	Renton Tao	NC Chen

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1. Introduction

1.1 Product Overview

AzureWave Technologies, Inc. introduces the IEEE 802.11ac/a/b/g/n 2X2 MU-MIMO WLAN & Bluetooth NGFF module --- **AW-CM276NF**. The module is targeted to mobile devices including **Notebook, TV, Tablet and Gaming Device** which need small package module, low power consumption, multiple interfaces and OS support. By using AW-CM276NF, the customers can easily enable the Wi-Fi, and BT embedded applications with the benefits of **high design flexibility, short development cycle, and quick time-to-market.**

Compliance with the IEEE 802.11ac/a/b/g/n standard supporting 802.11ac Wave 2, the AW-CM276NF uses Direct Sequence Spread Spectrum (**DSSS**), Orthogonal Frequency Division Multiplexing (**OFDM**), **DBPSK**, **DQPSK**, **CCK** and **QAM** baseband modulation technologies. A high level of integration and full implementation of the power management functions specified in the IEEE 802.11 standard minimize the system power requirements by using AW-CM276NF. In addition to the support of **WPA/WPA2/WPA3** and **WEP** 64-bit and 128-bit encryption, the AW-CM276NF also supports the **IEEE 802.11i** security standard through the implementation of **Advanced Encryption Standard** (**AES)/Counter Mode CBC-MAC Protocol (CCMP),** Wired Equivalent Privacy (**WEP)** with Temporal Key Integrity Protocol (**TKIP)**, Advanced Encryption Standard (**AES**)/Cipher-Based Message Authentication Code (**CMAC**), and WLAN Authentication and Privacy Infrastructure (**WAPI**) security mechanisms.

For the video, voice and multimedia applications the AW-CM276NF support **802.11e Quality of Service** (**QoS).** The device also supports **802.11h Dynamic Frequency Selection (DFS)** for detecting radar pulses when operating in the 5GHz range.

For Bluetooth operation, AW-CM276NF is **Bluetooth 5.1 (supports Low Energy).**

AW-CM276NF supports **PCIE and SDIO3.0** for WLAN and high speed **UART interfaces** for Bluetooth to the host processor.

AW-CM276NF is suitable for multiple mobile processors for different applications with the support cellular phone co-existence.

AW-CM276NF module adopts NXP's latest highly-integrated dual-band WLAN & Bluetooth SoC---**88W8997**. All the other components are implemented by all means to reach the mechanical specification required.

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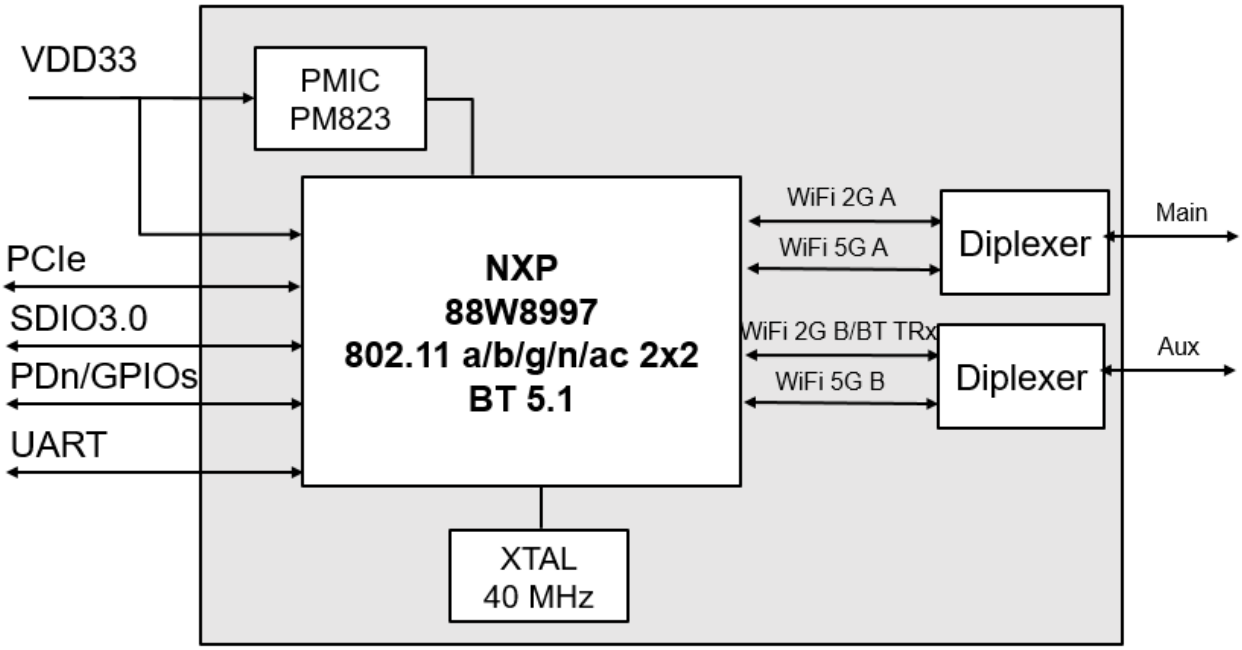
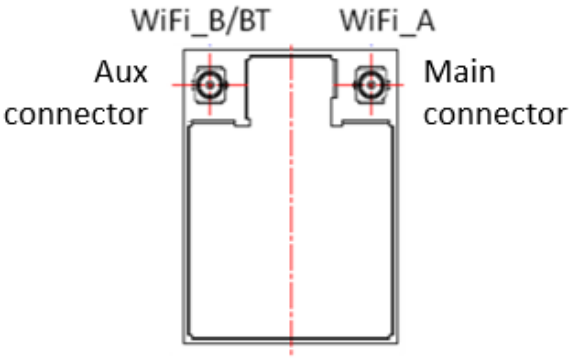
1.2. Block Diagram

AW-CM276NF NGFF Module



AW-CM276NF



Module antenna configuration

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1.3 Specifications Table

1.3.1 General

Features	Description
Product Description	IEEE 802.11 2X2 WiFi 5 MIMO Wireless LAN + Bluetooth 5.1 Combo LGA Module
Major Chipset	NXP 88W8997
Host Interface	WiFi + BT ● PCIe2.0 + UART ● SDIO3.0 + UART (For Host configuration interface, please refer to section 2.3)
Dimension	12 mm X 16 mm x 1.85 mm(Max) (Tolerance remarked in mechanical drawing)
Form factor	M.2 1216 130pins LGA package
Antenna	I-PEX MHF4 Connector Receptacle (20449) Main：WiFi → TX/RX Aux：WiFi/Bluetooth → TX/RX
Weight	0.5 g

1.3.2 WLAN

Features	Description
WLAN Standard	IEEE 802.11 a/b/g/n/ac
WLAN VID/PID	1B4B/2B42
WLAN SVID/SPID	N/A
Frequency Rage	2.4 GHz：2.412 ~ 2.484 GHz 5 GHz：4.915 ~5.925GHz
Modulation	DSSS, OFDM, DBPSK, DQPSK, CCK, 16-QAM, 64-QAM, 256-QAM
Number of Channels	**2.4GHz** ■ USA, NORTH AMERICA, Canada and Taiwan – 1 ~ 11 ■ China, Australia, Most European Countries, Japan – 1 ~ 13 **5GHz** ■ USA, EUROPE –36,40,44,48,52,56,60,64,100,104,108,112,116,120, 124,128,132,136,140,149,153,157,161,165

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Output Power (Board Level Limit)*

2.4GHz

	Min	Typ	Max	Unit
11b (11Mbps) @EVM<35%	15.5	17	18.5	dBm
11g (54Mbps) @EVM≦-27 dB	14.5	16	17.5	dBm
11n (HT20 MCS7) @EVM≦-28 dB	14.5	16	17.5	dBm
11n (HT40 MCS7) @EVM≦-28 dB	12.5	14	15.5	dBm

5GHz

	Min	Typ	Max	Unit
11a (54Mbps) @EVM≦-27 dB	11	13	15	dBm
11n (HT20 MCS7) @EVM≦-28 dB	11	13	15	dBm
11n (HT40 MCS7) @EVM≦-28 dB	10	12	14	dBm
11ac (VHT20 MCS8) @EVM≦-30 dB	11	13	15	dBm
11ac (VHT40 MCS9) @EVM≦-32 dB	10	12	14	dBm
11ac (VHT80 MCS9) @EVM≦-32 dB	8	10	12	dBm

Receiver Sensitivity

2.4GHz

	Min	Typ	Max	Unit
11b (11Mbps)		-88	-85	dBm
11g (54Mbps)		-75	-72	dBm
11n (HT20 MCS7)		-72	-70	dBm
11n (HT40 MCS7)		-69	-67	dBm

5GHz

	Min	Typ	Max	Unit
11a (54Mbps)		-72	-68	dBm
11n (HT20 MCS7)		-70	-67	dBm
11n (HT40 MCS7)		-68	-65	dBm
11ac(VHT20 MCS8)		-65	-62	dBm
11ac(VHT40 MCS9)		-63	-60	dBm
11ac(VHT80 MCS9)		-60	-57	dBm

Data Rate

- 802.11b: 1, 2, 5.5, 11Mbps
- 802.11a/g: 6, 9, 12, 18, 24, 36, 48, 54Mbps
- 802.11n: up to 150Mbps-single

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	■ 802.11n: up to 300Mbps-2x2 MIMO ■ 802.11ac:up to 192.6Mbps (20MHz channel) ■ 802.11ac:up to 400Mbps (40MHz channel) 802.11ac:up to 866.7Mbps (80MHz channel)
Security	■ WAPI ■ WEP 64-bit and 128-bit encryption with H/W TKIP processing ■ WPA/WPA2/WPA3 (Wi-Fi Protected Access) AES-CCMP hardware implementation as part of 802.11i security standard

* If you have any certification questions about output power please contact FAE directly.

1.3.3 Bluetooth

<table>
<tr><th>Features</th><th>Description</th></tr>
<tr><td>Bluetooth Standard</td><td>Bluetooth 2.1 and 3.0+Enhanced Data Rate (EDR) + BT 5.1</td></tr>
<tr><td>Bluetooth VID/PID</td><td>1286/204E</td></tr>
<tr><td>Frequency Rage</td><td>2402MHz~2480MHz</td></tr>
<tr><td>Modulation</td><td>Header GFSK
Payload 2M: π/4-DQPSK
Payload 3M: 8DPSK</td></tr>
<tr><td>Output Power</td><td>
<table>
<tr><td></td><td>Min</td><td>Typ</td><td>Max</td><td>Unit</td></tr>
<tr><td>BDR</td><td>0</td><td>2</td><td>4</td><td>dBm</td></tr>
<tr><td>EDR</td><td>0</td><td>2</td><td>4</td><td>dBm</td></tr>
<tr><td>BLE</td><td>0</td><td>2</td><td>4</td><td>dBm</td></tr>
</table>
</td></tr>
<tr><td>Receiver Sensitivity</td><td>
<table>
<tr><td></td><td>Min</td><td>Typ</td><td>Max</td><td>Unit</td></tr>
<tr><td>BDR</td><td></td><td>-83</td><td></td><td>dBm</td></tr>
</table>
</td></tr>
</table>

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1.3.4 Operating Conditions

Features	Description
Operating Conditions	
Voltage	3.3V+-5%
Operating Temperature	-30 ℃~ 85℃
Operating Humidity	less than 85% R.H.
Storage Temperature	-40 ℃~ 125℃
Storage Humidity	less than 60% R.H.
ESD Protection	
Human Body Model	+-2kV
Changed Device Model	+-500V

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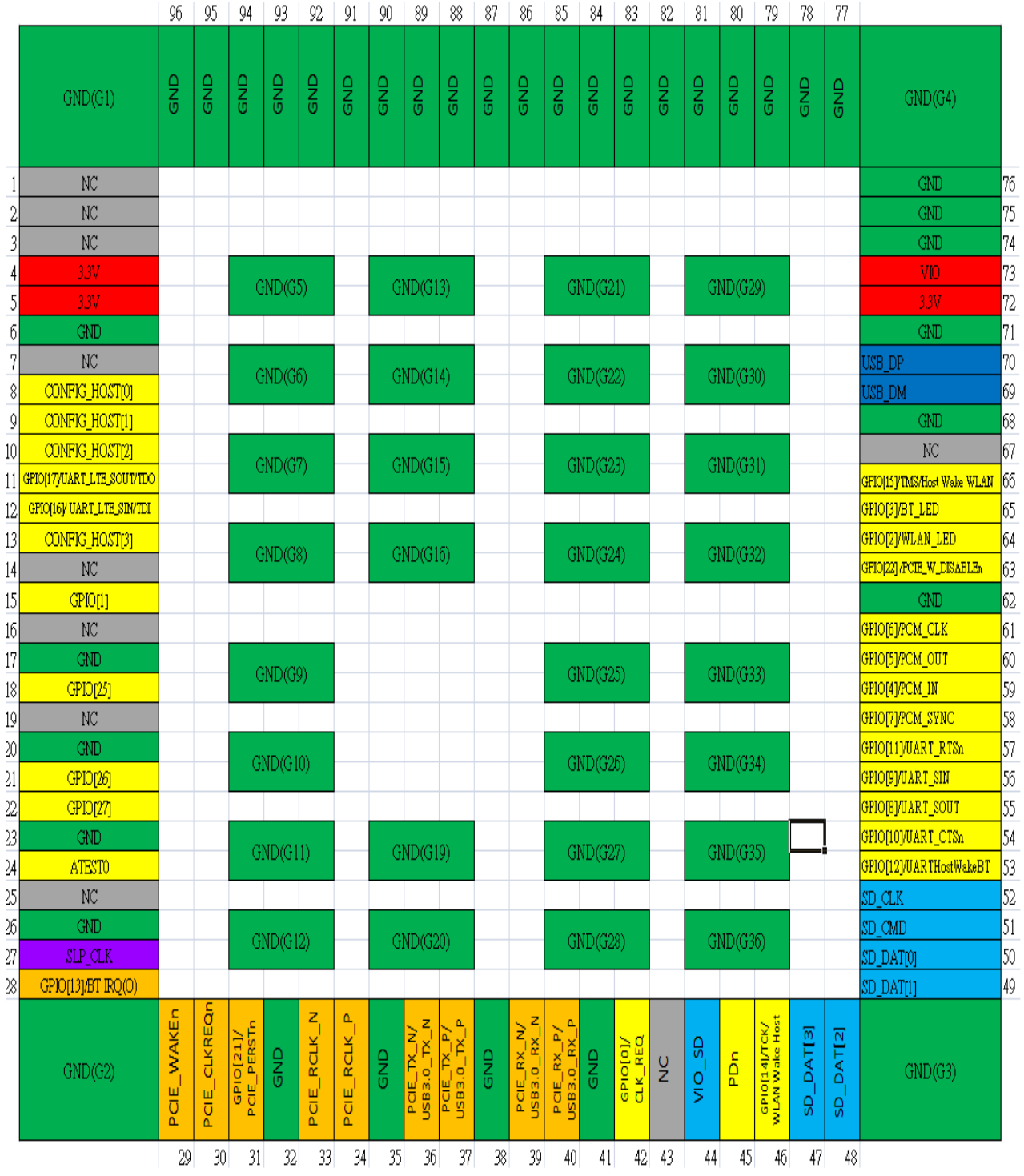
2. Pin Definition

2.1. Pin map



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2.2. Pin Table

Pin No	Definition	Basic Description	Voltage	Type
1	NC	NC		
2	NC	NC		
3	NC	NC		
4	3.3V	3.3V Power Supply	3.3V	I
5	3.3V	3.3V Power Supply	3.3V	I
6	GND	System Ground Pin		GND
7	NC	NC		
8	CONFIG_HOST[0]	Configuration: CONFIG_HOST[0]		
9	CONFIG_HOST[1]	Configuration: CONFIG_HOST[1]		
10	CONFIG_HOST[2]	Configuration: CONFIG_HOST[2]		
11	GPIO[17] /UART_LTE_SOUT/TDO	GPIO[17] / UART_LTE_SOUT/TDO (output)	VIO	O
12	GPIO[16]/ UART_LTE_SIN/TDI	GPIO[16] / UART_LTE_SIN/TDI (input)	VIO	I
13	CONFIG_HOST[3]	Configuration: CONFIG_HOST[3]		
14	NC	NC		
15	GPIO[1]	GPIO[1] (input/output)	VIO	I/O
16	NC	NC		I/O
17	GND	System Ground Pin		GND
18	GPIO[25]	GPIO[25] (input/output)	VIO	I/O
19	NC	NC		
20	GND	System Ground Pin		GND
21	GPIO[26]	GPIO[26] (input/output)	VIO	I/O
22	GPIO[27]	GPIO[27] (input/output)	VIO	I/O
23	GND	System Ground Pin		
24	ATEST0	NC, reserved for debug		I
25	NC	NC		I/O
26	GND	System Ground Pin		GND
27	SLP_CLK	Sleep Clock Input Used for WLAN and Bluetooth low-power modes. External sleep clock of 32.768 KHz must be used for auto reference clock calibration and for WLAN/Bluetooth low power operation.		I
28	GPIO[13]/BT IRQ(O)	GPIO[13]/ BT Wake Host(active low) (output)	VIO	O
29	PCIE_WAKEn	PCIe wake signal (input/output) (active low)	VIO	I/O
30	PCIE_CLKREQn	PCIe clock request (input/output) (active low)	VIO	I/O
31	GPIO[21]/PCIE_PERSTn	PCIe host indication to reset the device (input) (active low)	VIO	I
32	GND	System Ground Pin		GND
33	PCIE_RCLK_N	PCI Express Differential Clock Input—Negative	1.8V(internal)	I
34	PCIE_RCLK_P	PCI Express Differential Clock Input—Positive	1.8V(internal)	I
35	GND	System Ground Pin		GND
36	PCIE_TX_N/USB3.0_TX_N	PCI Express Transmit Data—Negative / USB 3.0 TX negative	1.8V(internal)	O
37	PCIE_TX_P/USB3.0_TX_P	PCI Express Transmit Data—Positive / USB 3.0 TX positive	1.8V(internal)	O
38	GND	System Ground Pin		GND
39	PCIE_RX_N/USB3.0_RX_N	PCI Express Receive Data—Negative / USB 3.0 RX negative	1.8V(internal)	I
40	PCIE_RX_P/USB3.0_RX_P	PCI Express Receive Data—Positive / USB 3.0 RX positive	1.8V(internal)	I
41	GND	System Ground Pin		GND
42	GPIO[0]/CLK_REQ	GPIO[0] (input/output)	VIO	O

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43	NC	NC		
44	VIO_SD	1.8V/3.3V Digital I/O SDIO Power Supply	VIO_SD	I
45	PDn	Full Power Down (input) (active low)	3.3V	I
46	GPIO[14] /TCK/WLAN Wake Host	GPIO[14]/TCK/WLAN Wake Host(active low) (output)	VIO	O
47	SD_DAT[3]	SDIO Data line Bit[3]	VIO_SD	I/O
48	SD_DAT[2]	SDIO Data line Bit[2]	VIO_SD	I/O
49	SD_DAT[1]	SDIO Data line Bit[1]	VIO_SD	I/O
50	SD_DAT[0]	SDIO Data line Bit[0]	VIO_SD	I/O
51	SD_CMD	SDIO Command/response (input/output)	VIO_SD	I/O
52	SD_CLK	SDIO Clock input	VIO_SD	I
53	GPIO[12] / UART Host Wake BT	GPIO[12]/ UART Host Wake BT(active low) (input)	VIO	I
54	GPIO[10] / UART_CTSn	GPIO[10 / UART_CTSn] (input)	VIO	I
55	GPIO[8] / UART_SOUT	GPIO[8] / UART_SOUT (output)	VIO	O
56	GPIO[9] / UART_SIN	GPIO[9] / UART_SIN (input)	VIO	I
57	GPIO[11] / UART_RTSn	GPIO[11] / UART_RTSn (output)	VIO	O
58	GPIO[7] / PCM_SYNC	GPIO[7] / PCM_SYNC (input/output)	VIO	I/O
59	GPIO[4] / PCM_IN	GPIO[4] / PCM_IN (input)	I	VIO
60	GPIO[5] / PCM_OUT	GPIO[5] / PCM_OUT (output)	O	VIO
61	GPIO[6] / PCM_CLK	GPIO[6] / PCM_CLK (input)	I	VIO
62	GND	System Ground Pin		GND
63	GPIO[22] / PCIE_W_DISABLEn	GPIO[22] / PCIE_W_DISABLEn (input)	I	VIO
64	GPIO[2] / WLAN_LED	LED_OUT_WLAN (output)	O	VIO
65	GPIO[3] / BT_LED	LED_OUT_BT (output)	O	VIO
66	GPIO[15] / TMS/ Host Wake WLAN	GPIO[15] / JTAG TMS/ Host Wake WLAN (input)	I	VIO
67	NC	NC		
68	GND	System Ground Pin		GND
69	USB_DM	USB Serial Differential Data Minus	I/O	3.3V
70	USB_DP	USB Serial Differential Data Plus	I/O	3.3V
71	GND	System Ground Pin		GND
72	3.3V	3.3V Power Supply	I	3.3V
73	VIO	Digital I/O Power Supply	I	VIO
74	GND	System Ground Pin		
75	GND	System Ground Pin		
76	GND	System Ground Pin		
77	GND	System Ground Pin		
78	GND	System Ground Pin		
79	GND	System Ground Pin		
80	GND	System Ground Pin		
81	GND	System Ground Pin		

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82	GND	System Ground Pin		
83	GND	System Ground Pin		
84	GND	System Ground Pin		
85	GND	System Ground Pin		
86	GND	System Ground Pin		
87	GND	System Ground Pin		
88	GND	System Ground Pin		
89	GND	System Ground Pin		
90	GND	System Ground Pin		
91	GND	System Ground Pin		
92	GND	System Ground Pin		
93	GND	System Ground Pin		
94	GND	System Ground Pin		
95	GND	System Ground Pin		
96	GND	System Ground Pin		
G1~G36	GND	System Ground Pin		

Notes:

1. PCIE Impedance targets: Single-ended Z of 60 ohms +- 15% . Differential Impedance of ~100 ohm +- 20%.
2. USB Impedance targets: D+/D- are differential and should have 90ohms impedance.
3. * Implement by different hardware version.

Note: Interface supports and combinations as shown below:

Scenario	WLAN	BT	Strap value, CON[2:0]
1	SDIO	UART	000
2	reserved	reserved	001
3	reserved	reserved	010
4	PCIe	UART	011
5	reserved	reserved	100
6	reserved	reserved	101
7	reserved	reserved	110
8	reserved	reserved	111

*Configuration pins:

Pin No.	Configuration
10	CON[2]
9	CON[1]
8	CON[0]

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3. Electrical Characteristics

3.1 Absolute Maximum Ratings

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
Pin73/ VIO	Host I/O power supply	-- -- --	-- -- --	1.8 2.5 3.3	2.2 3.0 4.0	V
Pin44/ VIO_SD	SDIO power supply	-- --	-- --	1.8 3.3	2.2 4.0	
Pin4,5,72/ 3.3V	3.3V VBAT input	-	-	3.3	3.63	V
Tstorage	Storage Temperature	-	-40	-	125	℃

3.2 Recommended Operating Conditions

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Units
Pin73/ VIO	1.8V/2.5V/3.3V digital I/O power supply	-- -- --	1.62 2.25 2.97	1.8 2.5 3.3	1.98 2.75 3.63	V
Pin44/ VIO_SD	1.8V/3.3V digital I/O SDIO power supply	-- --	1.62 2.97	1.8 3.3	1.98 3.63	V
Pin4,5,72/ 3.3V	3.3V VBAT input	--	3.14	3.14	3.3	V
T_A	Ambient operating temperature	--	-30		85	℃

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3.3 Digital IO Pin DC Characteristics

3.3.1 DC Electricals-1.8V Operation (VIO)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{IH}	Input high voltage	0.7*VIO	-	VIO+0.4	V
V_{IL}	Input low voltage	-0.4	-	0.3*VIO	
V_{OH}	Output high voltage	VIO-0.4	-	-	
V_{OL}	Output low voltage	-	-	0.4	
V_{HYS}	Input Hysteresis	100			mV

3.3.2 3.3V Operation (VIO)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{IH}	Input high voltage	0.7*VIO	-	VIO+0.4	V
V_{IL}	Input low voltage	-0.4	-	0.3*VIO	
V_{OH}	Output High Voltage	VIO-0.4	-	-	
V_{OL}	Output Low Voltage	-	-	0.4	
V_{HYS}	Input Hysteresis	100			mV

3.3.3 1.8V Operation (VIO_SD)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{IH}	Input high voltage	0.7*VIO_SD	-	VIO_SD+0.4	V
V_{IL}	Input low voltage	-0.4	-	0.3*VIO_SD	
V_{OH}	Output High Voltage	VIO_SD-0.4	-	-	
V_{OL}	Output Low Voltage	-	-	0.4	
V_{HYS}	Input Hysteresis	100			mV

3.3.4 3.3V Operation (VIO_SD)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{IH}	Input high voltage	0.7*VIO_SD	-	VIO_SD+0.4	V
V_{IL}	Input low voltage	-0.4	-	0.3* VIO_SD	
V_{OH}	Output High Voltage	VIO_SD-0.4	-	-	
V_{OL}	Output Low Voltage	-	-	0.4	
V_{HYS}	Input Hysteresis	100			mV

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3.4 Host Interface

3.4.1. SDIO Interface

The AW-CM276NF supports a SDIO device interface that conforms to the industry standard SDIO Full-Speed card specification and allows a host controller using the SDIO bus protocol to access the Wireless module device.

The AW-CM276NF acts as the device on the SDIO bus. The host unit can access registers of the SDIO interface directly and can access shared memory in the device through the use of BARs and a DMA engine.

The SDIO device interface main features include:

Supports SDIO 3.0 Standard

On-chip memory used for CIS

Supports SPI, 1-bit SDIO, and 4-bit SDIO transfer modes

Special interrupt register for information exchange

Allows card to interrupt host

3.4.1.1. SDIO Interface Signal Description

Pin Name	Signal Name	Type	Description
SD_CLK	CLK	I/O	SDIO 1-bit mode: Clock SDIO SPI mode: Clock
SD_CMD	CMD	I/O	SDIO 1-bit mode: Command line SDIO SPI mode: Data input
SD_DAT[3]	DAT3	I/O	SDIO 4-bit mode: Data line bit [3] SDIO 1-bit mode: Not used SDIO SPI mode: Chip select (active low)
SD_DAT[2]	DAT2	I/O	SDIO 4-bit mode: Data line bit [2] or Read Wait (optional) SDIO 1-bit mode: Read Wait (optional) SDIO SPII mode: Reserved
SD_DAT[1]	DAT1	I/O	SDIO 4-bit mode: Data line bit [1] SDIO 1-bit mode: Interrupt SDIO SPI mode: Interrupt

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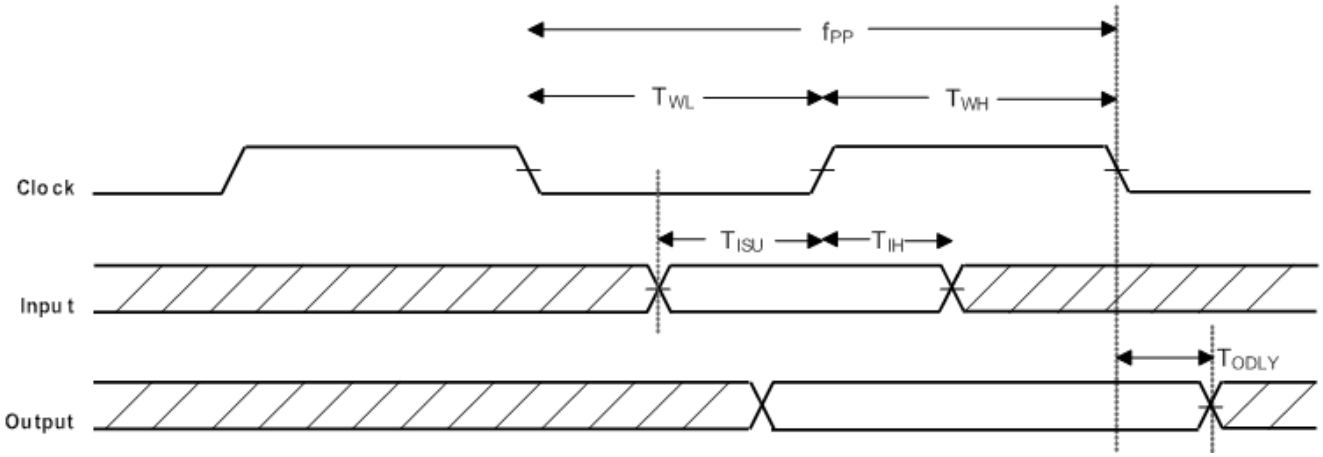
SD_DAT[0]	DAT0	I/O	SDIO 4-bit mode: Data line bit [0] SDIO 1-bit mode: Data line SDIO SPI mode: Data output

3.4.1.2. Default Speed, High Speed Modes (3.3V)

SDIO Protocol Timing Diagram – Default Speed Mode (3.3V)



SDIO Protocol Timing Diagram – HighSpeed Mode (3.3V)

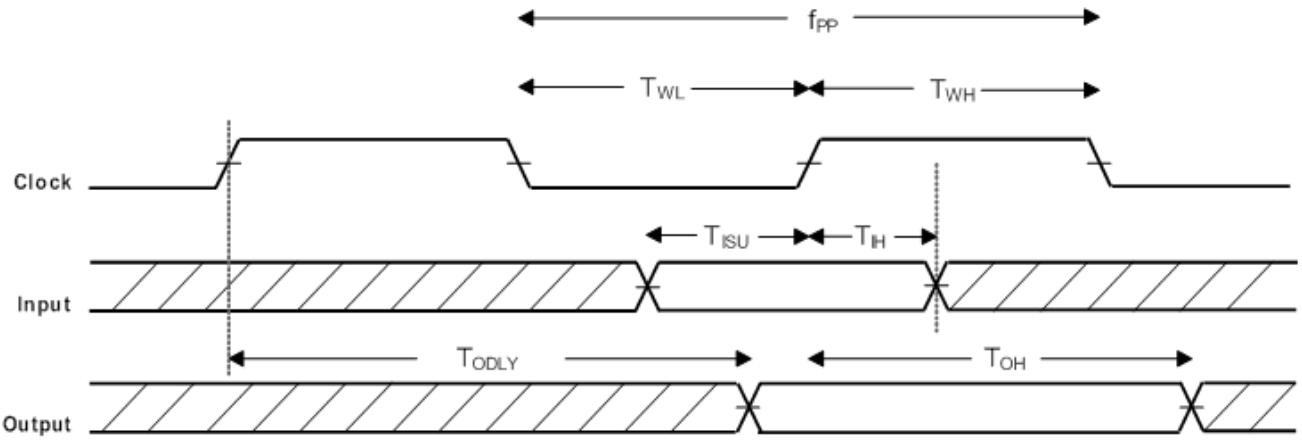


Table shows SDIO Timing Data—Default Speed, High Speed Modes (3.3V)

NOTE: Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

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Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{PP}	Clock Frequency	Default Speed	0	--	25	MHz
		High Speed	0	--	50	MHz
T_{WL}	Clock Low Time	Default Speed	10	--	--	ns
		High Speed	7	--	--	ns
T_{WH}	Clock High Time	Default Speed	10	--	--	ns
		High Speed	7	--	--	ns
T_{ISU}	Input Setup Time	Default Speed	5	--	--	ns
		High Speed	6	--	--	ns
T_{IH}	Input Hold Time	Default Speed	5	--	--	ns
		High Speed	2	--	--	ns
T_{ODLY}	Output Delay Time CL ≤ 40 pF (1 card)	Default Speed	--	--	14	ns
		High Speed	---	-1	4	ns
T_{OH}	Output Hold Time	High Speed	2.5	--	--	ns

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3.4.1.3. SDR12, SDR25, SDR50 Modes (up to 100MHz) (1.8V)

SDIO Protocol Timing Diagram – SDR12,SDR25,SDR50 Modes (up to 100MHz) (1.8V)

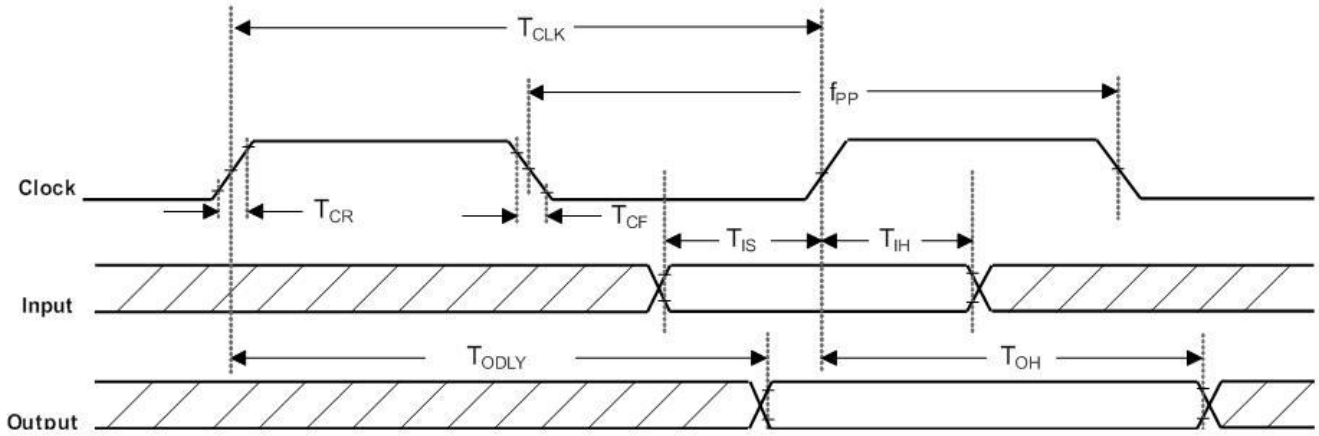

Table shows SDIO Timing Data—SDR12,SDR25,SDR50 Modes (up to 100MHz) (1.8V)

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{PP}	Clock frequency	SDR12/25/50	25	--	100	MHz
T_{IS}	Input setup time	SDR12/25/50	3	--	--	ns
T_{IH}	Input hold time	SDR12/25/50	0.8	--	--	ns
T_{CLK}	Clock time	SDR12/25/50	10	--	40	ns
T_{CR}, T_{CF}	Rise time, fall time T_{CR}, T_{CF} < 2 ns (max) at 100 MHz C_{CARD} = 10 pF	SDR12/25/50	--	--	0.2*T_{CLK}	ns
T_{ODLY}	Output delay time C_L ≤ 30 pF	SDR12/25/50	--	--	7.5	ns
T_{OH}	Output hold time C_L = 15 pF	SDR12/25/50	1.5	--	--	ns

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3.4.1.4. SDR104 Modes (208MHz) (1.8V)

SDIO Protocol Timing Diagram –SDR104 Mode (208MHz)

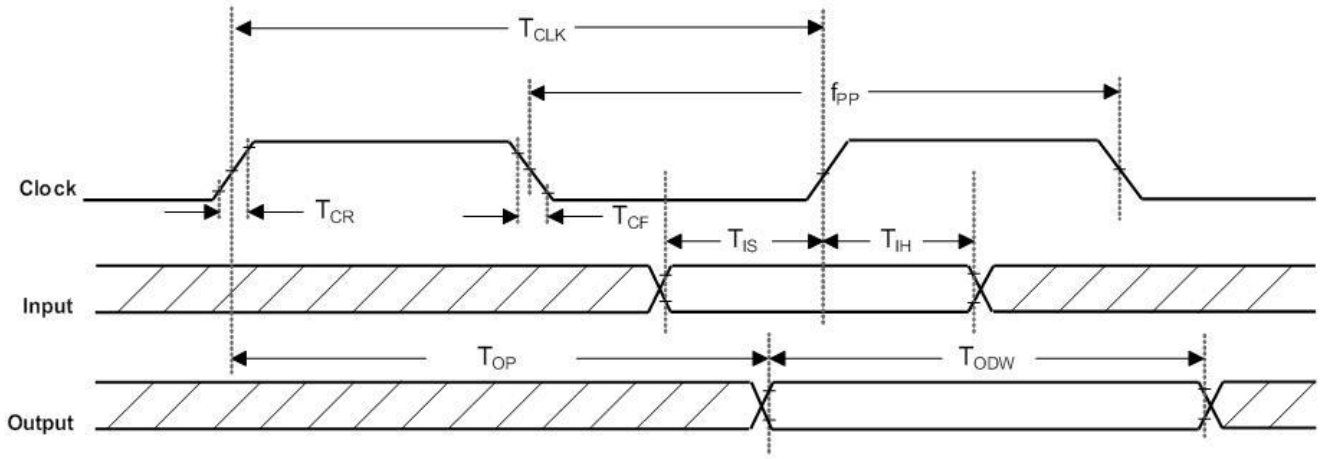

Table shows SDIO Timing Data—SDR104 Mode (208MHz)

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{PP}	Clock frequency	SDR104	0	--	208	MHz
T_{IS}	Input setup time	SDR104	1.4	--	--	ns
T_{IH}	Input hold time	SDR104	0.8	--	--	ns
T_{CLK}	Clock time	SDR104	4.8	--	--	ns
T_{CR}, T_{CF}	Rise time, fall time T_{CR}, T_{CF} < 0.96 ns (max) at 208 MHz C_{CARD} = 10 pF	SDR104	--	--	0.2*T_{CLK}	ns
T_{OP}	Card output phase	SDR104	0	--	10	ns
T_{ODW}	Output timing of variable data window	SDR104	2.88	--	--	ns

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3.4.2. PCI Express Interface

3.4.2.1. Differential Tx Output Electricals

Symbol	Parameter	Min	Typ	Max	Units
UI	Unit interval Each UI is 400 ps ±300 PPM. UI does not account for SSC dictated variations.	399.98	400	400.12	ps
V_{Tx_DIFFpp}	Differential peak-to-peak output voltage $V_{Tx_DIFFpp} = 2*\|V_{TX-D+} - V_{TX-D-}\|$	0.800	--	1.2	V
$V_{Tx_DE_RATIO}$	De-emphasized differential output voltage (ratio)	-3.0	-3.5	-4.0	db
T_{Rx_EYE}	Minimum Tx eye width	0.75	--	--	UI
$T_{Rx_EYE_MEDIAN_MAX_JIT}$	Maximum time between jitter median and maximum deviation from median	--	--	0.125	UI
T_{Tx_RISE}, T_{Tx_FALL}	D+/D- Tx output rise/fall time	0.125	--	--	UI
$V_{Tx_CM_DC_ACTIVE_IDLE_DELTA}$	Absolute delta of DC common mode voltage during L0 and electrical idle	0-	-	100	mV
$V_{Tx_CM_DC_LINE_DELTA}$	Absolute delta of DC common mode voltage between D+ and D-	0-	-	25	mV
$V_{Tx_IDLE_DIFFp}$	Electrical idle differential peak output voltage	0	--	20	mV
$V_{Tx_RCV_DETECT}$	Voltage change allowed during receiver detection	--	--	600	mV
$V_{Tx_DC_CM}$	Tx DC common mode voltage	--	--	3.6	V
I_{Tx_SHORT}	Tx short circuit current limit	--	--	90	mA
$T_{Tx_IDLE_MIN}$	Minimum time spent in electrical idle	50	--	--	UI
$T_{Tx_IDLE_SET_TO_IDLE}$	Maximum time to transition to a valid electrical idle after sending an electrical idle ordered set	--	--	20	UI
$T_{Tx_IDLE_TO_DIFF_DATA}$	Maximum time to transition to valid Tx specifications after leaving an electrical idle condition	--	--	20	UI
RL_{Tx_DIFF}	Differential return loss	10	--	--	dB
RL_{Tx_CM}	Common mode return loss	6	--	--	dB
C_{Tx}	AC coupling capacitor	75	--	200	nF
$T_{Crosstalk}$	Crosstalk random timeout	0	--	1	ms

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3.4.2.2. Differential Rx Output Electricals

Symbol	Parameter	Min	Typ	Max	Units
UI	Unit interval Each UI is 400 ps ±300 ppm. UI does not account for SSC dictated variations.	399.98	400	400.12	ps
V_{Rx_DIFFpp}	Differential peak-to-peak voltage $V_{Rx_DIFFpp} = 2*\|V_{RX-D+} - V_{RX-D-}\|$	0.175	--	1.2	V
T_{Rx_EYE}	Minimum receiver eye width	0.4	--	--	UI
$T_{Rx_EYE_MEDIAN_MAX_JIT}$	Maximum time between jitter median and maximum deviation from median	--	--	0.3	UI
$V_{Rx_CM_ACp}$	AC peak common mode input voltage	--	--	150	mV
RL_{Rx_DIFF}	Differential return loss	10	--	--	dB
RL_{Rx_CM}	Common mode return loss	6	--	--	dB
$Z_{Rx_DIFF_DC}$	DC differential input impedance	80	100	120	Ω
Z_{Rx_DC}	DC input impedance	40	50	60	Ω
$Z_{Rx_HIGH_IMP_DC_POS}$	Powered down DC input impedance positive	50	--	--	k
$Z_{Rx_HIGH_IMP_DC_NEG}$	Powered down DC input impedance negative	1	--	--	kΩ
$V_{Rx_IDLE_DET_DIFFpp}$	Electrical idle detect threshold	65	--	175	mV
$T_{Rx_IDLE_DET_DIFF_ENTERTIME}$	Unexpected electrical idle enter detect threshold integration time	--	--	10	ms
L_{Rx_SKEW}	Total skew	---	-2	0	ns

3.4.3. USB Interface

The USB device interface is compliant with the Universal Serial Bus Specification, Revision 2.0, April 27, 2000. A USB host uses the USB cable bus and the USB 2.0 device interface to communicate with the chip.

The main features of the USB device interface include:

High/full speed operation (480/12 Mbps)

Suspend/host resume/device resume (remote wake-up)

Built-in DMA engine that reduces interrupt loads on the embedded processor and reduces the system bus bandwidth requirement for serving the USB device operation

The USB 2.0 device interface is designed with 3.3V signal level pads.

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3.4.3.1. USB 2.0 Device Interface Description

Table shows the signal mapping between the AW-CM276NF and the USB Specification, Revision 2.0.

Pin Name	USB 2.0 Specification Pin Name	Description
Pin72/ 3V3_USB	VBUS	USB Bus Power Supply On-board regulator regulates voltage from VBUS level to voltage levels used by USB PHY.
	GND	USB Bus Ground Common ground on SoC device.
Pin70/ USB_DP	D+	USB Bus Data Positive. One of the differential data pair.
Pin69/ USB_DN	D-	USB Bus Data Negative. One of the differential data pair.

3.4.3.2. USB 2.0 Device Functional Description

The device controller uses internal Scatter/Gather DMA engine to transfer the transmit packet from internal SRAM to USB and the receive packet from USB to internal SRAM. The Device IN Endpoint DMA (DIEPDMAn) and Device OUT Endpoint DMA (DOEPDMAn) registers are used by the DMA engine to access the base descriptor. The application is interrupted after the programmed transfer size extracted from the descriptors is transmitted or received. By using registers, interrupts, and special data structures, the device controller can communicate with the device controller driver (application/software) about bus states, host request, and data transfer status. The device controller driver also has all of the routines to respond to the device framework commands issued by a USB host, so it controls the attachment, configuration, operation, and detachment of the device.

3.4.4. High-Speed UART Interface

The AW-CM276NF supports a high-speed Universal Asynchronous Receiver/Transmitter (UART) interface, compliant to the industry standard 16550 specification. High-speed baud rates are supported to provide the physical transport between the device and the host for exchanging Bluetooth data. Table shows the rates supported.

The UART interface features include:

FIFO mode permanently selected for transmit and receive operations

Two pins for transmit and receive operations

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Two flow control pins

Interrupt triggers for low-power, high throughput operation

The UART interface operation includes:

Upload boot code to the internal CPU (for debug purposes)

Support diagnostic tests

Support data input/output operations for peripheral devices connected through a standard UART interface

UART Baud Rates Supported

Baud Rate				
1200	38400	460800	1500000	3000000
2400	57600	500000	1843200	3250000
4800	76800	921600	2000000	3692300
9600	115200	1000000	2100000	4000000
19200	230400	1382400	2764800	--

3.4.4.1. UART Interface Signal Description

Table shows the standard UART signal names on the device.

Signal Name	16550 Standard Pin Name	Description
Data Bus		
UART_SIN	SIN	Serial data input from modem, data set, or peripheral device
UART_SOUT	SOUT	Serial data output from modem, data set, or peripheral device
Modem Control		
UART_RTSN	RTS	Request To Send output to modem, data set, or peripheral device (active low)
UART_CTSN	CTS	Clear To Send input from modem, data set, or peripheral device (active low)

3.4.4.2. UART Interface Functional Description

3.4.4.2.1. Booting from UART

When booting from the UART, the AW-CM276NF device has the following requirements:

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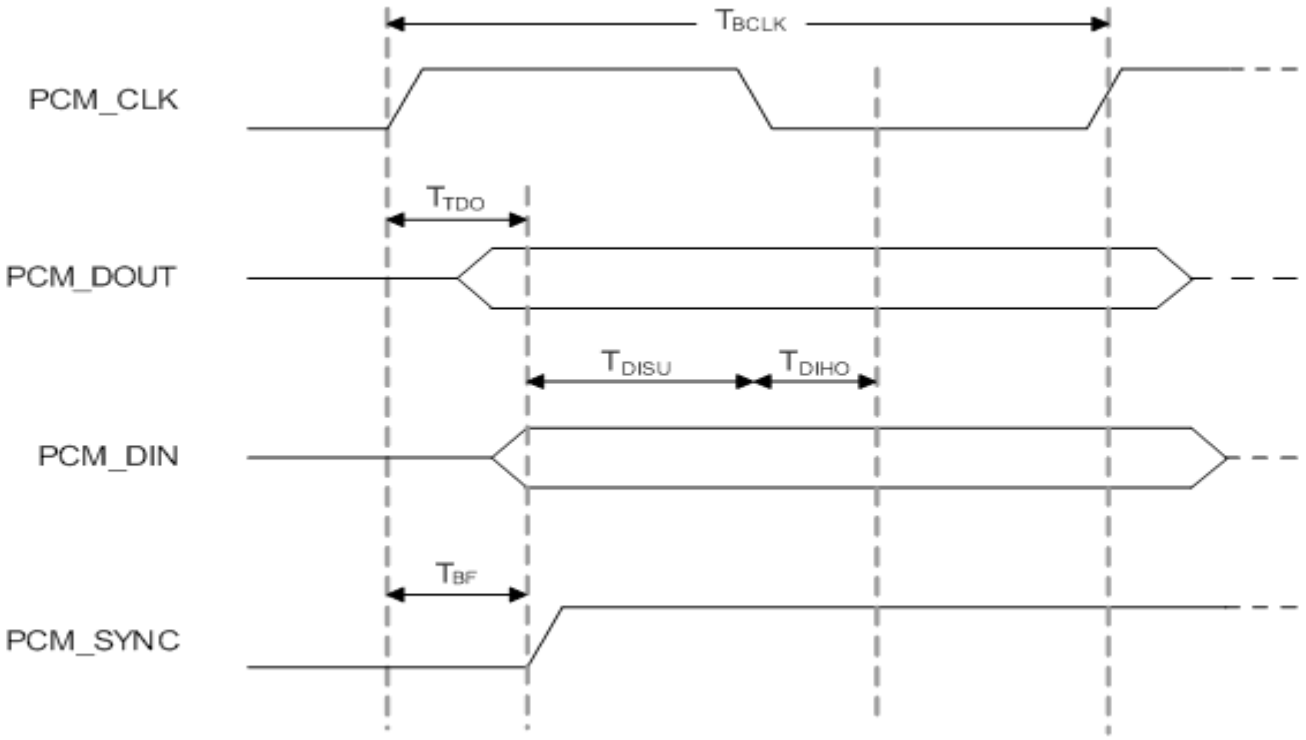
System Requirement	Description
Number of data bits	8 bits
Stop bits	1 bit
Parity	No parity
Baud Rate	115200

3.4.4.2.2. UART as Test Port

Test diagnostic programs may be uploaded to the CPU through the UART interface. During execution, the diagnostic program transmits performance and status information through the UART by performing a write to the PBU address space designated to the UART.

3.4.5. PCM Interface

3.4.5.1. PCM Timing Specification – Master Mode



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Symbol	Parameter	Condition	Min	Typ	Max	Units
F_{BCLK}	--	--	--	2/2.048	--	MHz
Duty $Cycle_{BCLK}$	--	--	0.4	0.5	0.6	--
$T_{BCLK\ rise/fall}$	--	--	--	3	--	ns
T_{DO}	--	--	--	--	15	ns
T_{DISU}	--	--	20	--	--	ns
T_{DIHO}	--	--	15	--	--	ns
T_{BF}	--	--	--	--	15	ns

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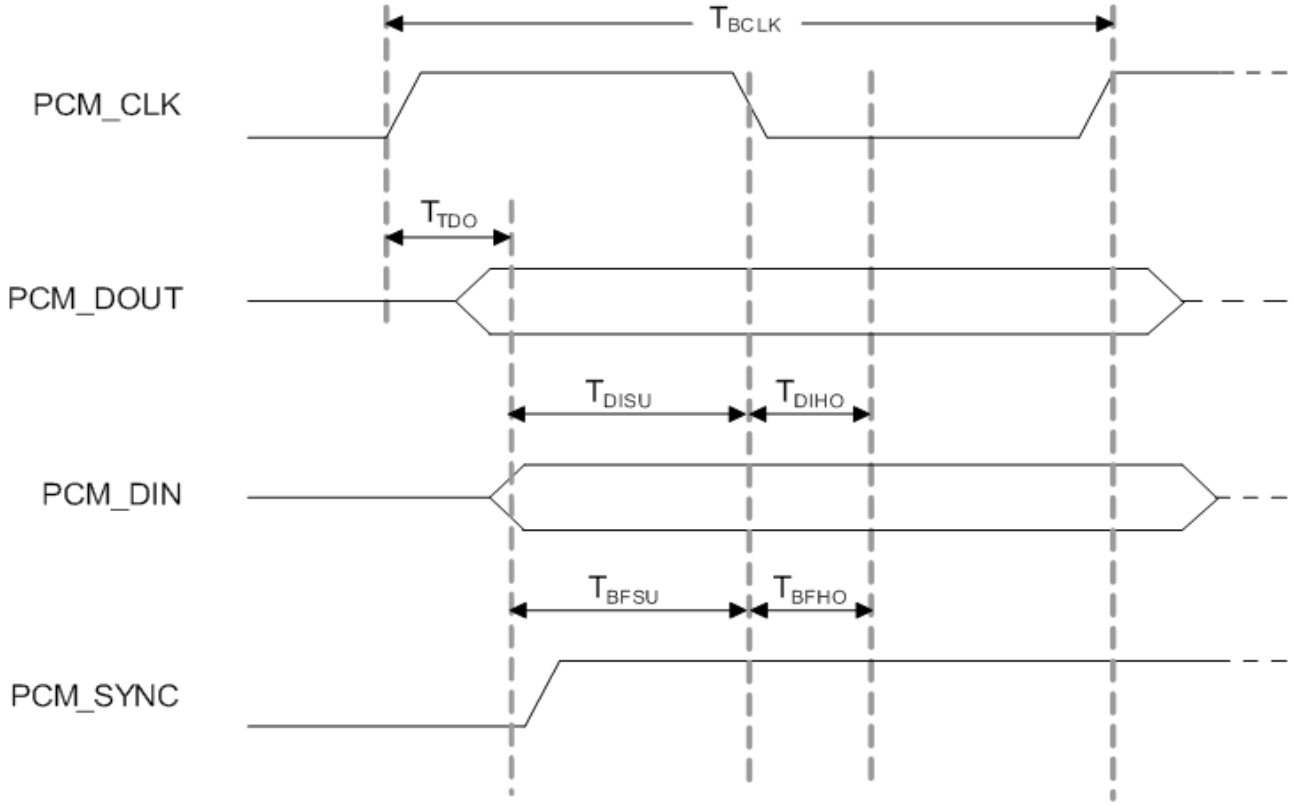
3.4.5.2. PCM Timing Specification – Slave Mode



Symbol	Parameter	Condition	Min	Typ	Max	Units
F_{BCLK}	--	--	--	2/2.048	--	MHz
Duty $Cycle_{BCLK}$	--	--	0.4	0.5	0.6	--
$T_{BCLK\ rise/fall}$	--	--	--	3	--	ns
T_{DO}	--	--	--	--	30	ns
T_{DISU}	--	--	15	--	--	ns
T_{DIHO}	--	--	10	--	--	ns
T_{BFSU}	--	--	15	--	--	ns
T_{BFHO}	--	--	10	--	--	ns

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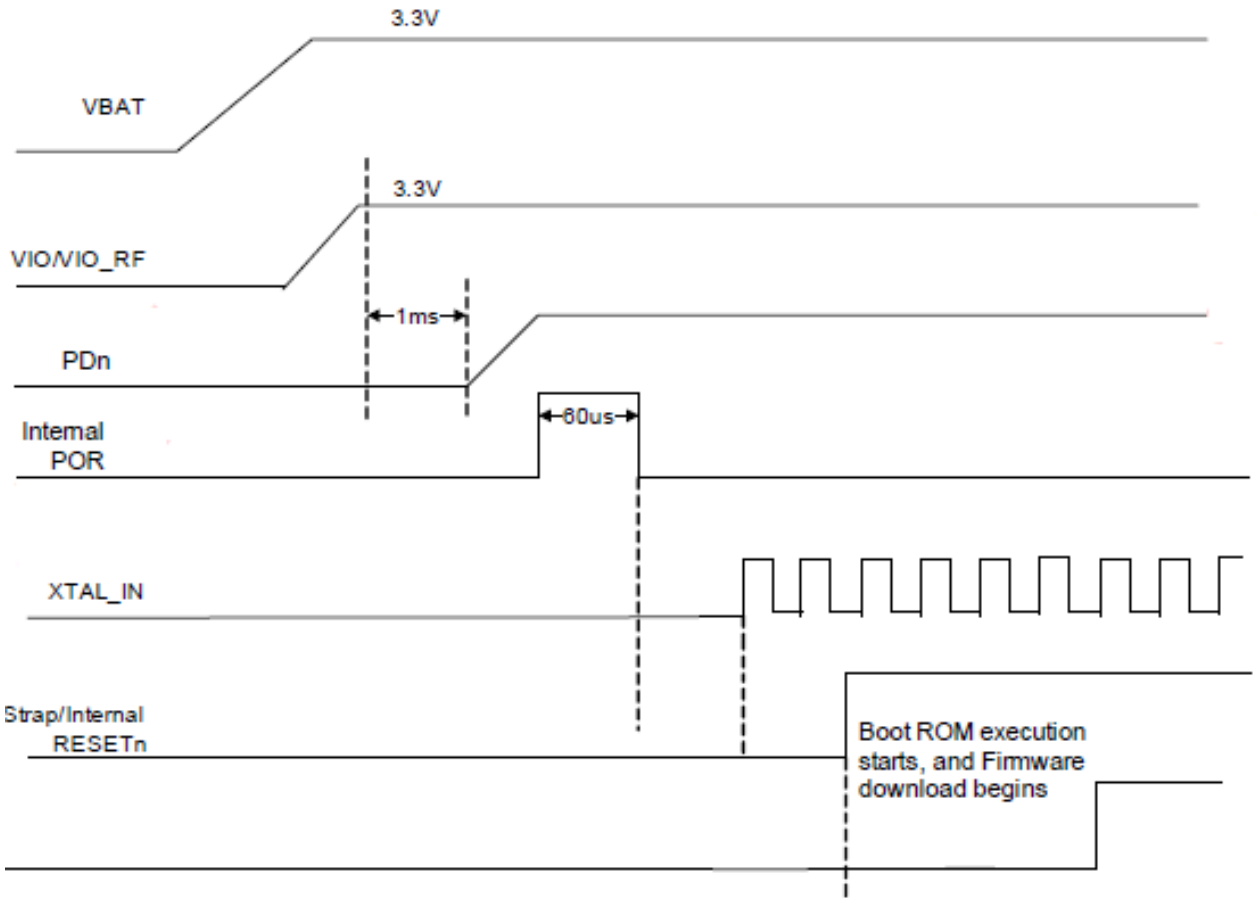
3.5. Power up Timing Sequence



3.5.1. Reset Configuration

The AW-CM276NF is reset to its default operating state under the following conditions:

- Power-on reset (POR)
- Software/Firmware reset
- External pin for power down (PDn)

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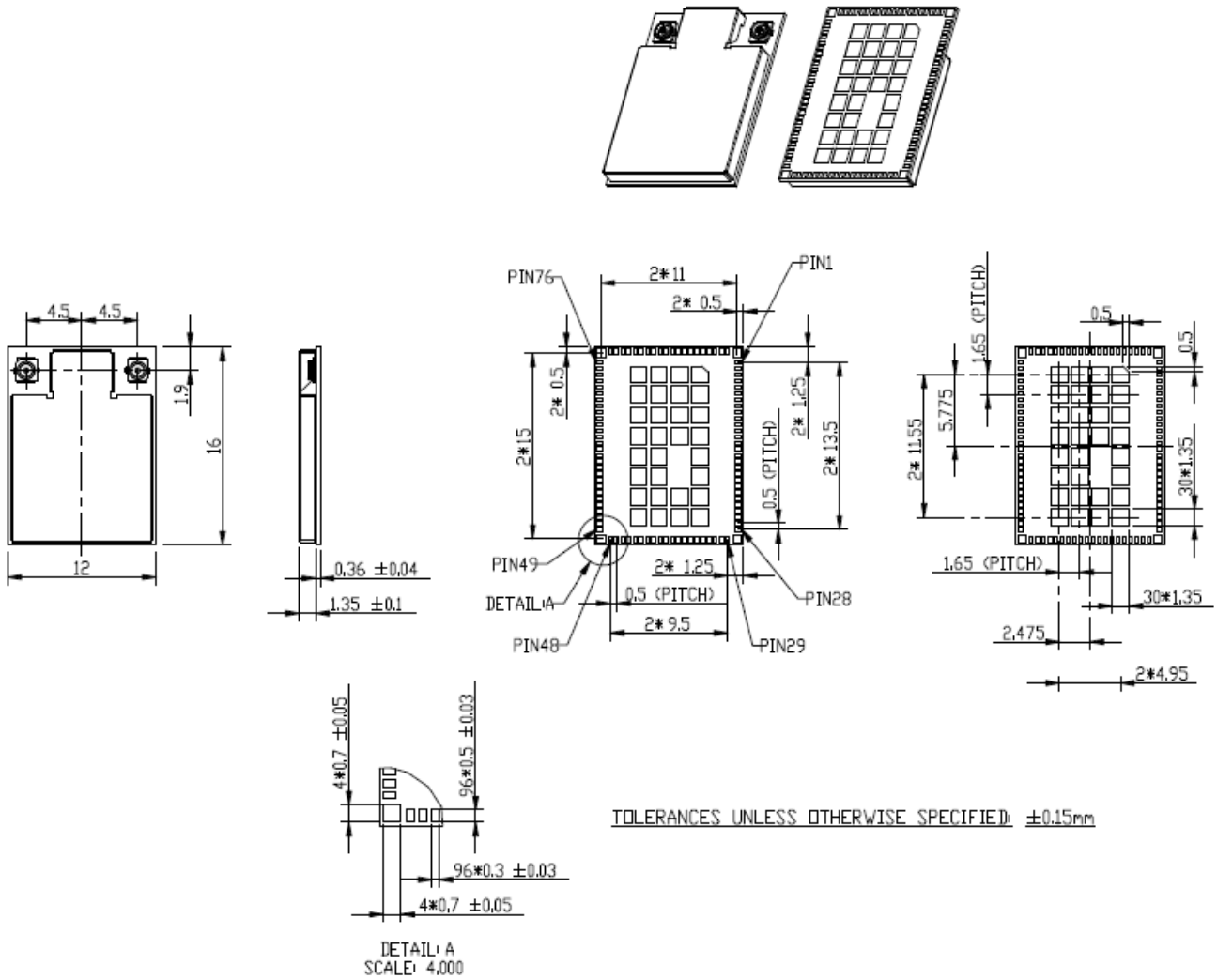
4. Mechanical Information

4.1 Mechanical Drawing



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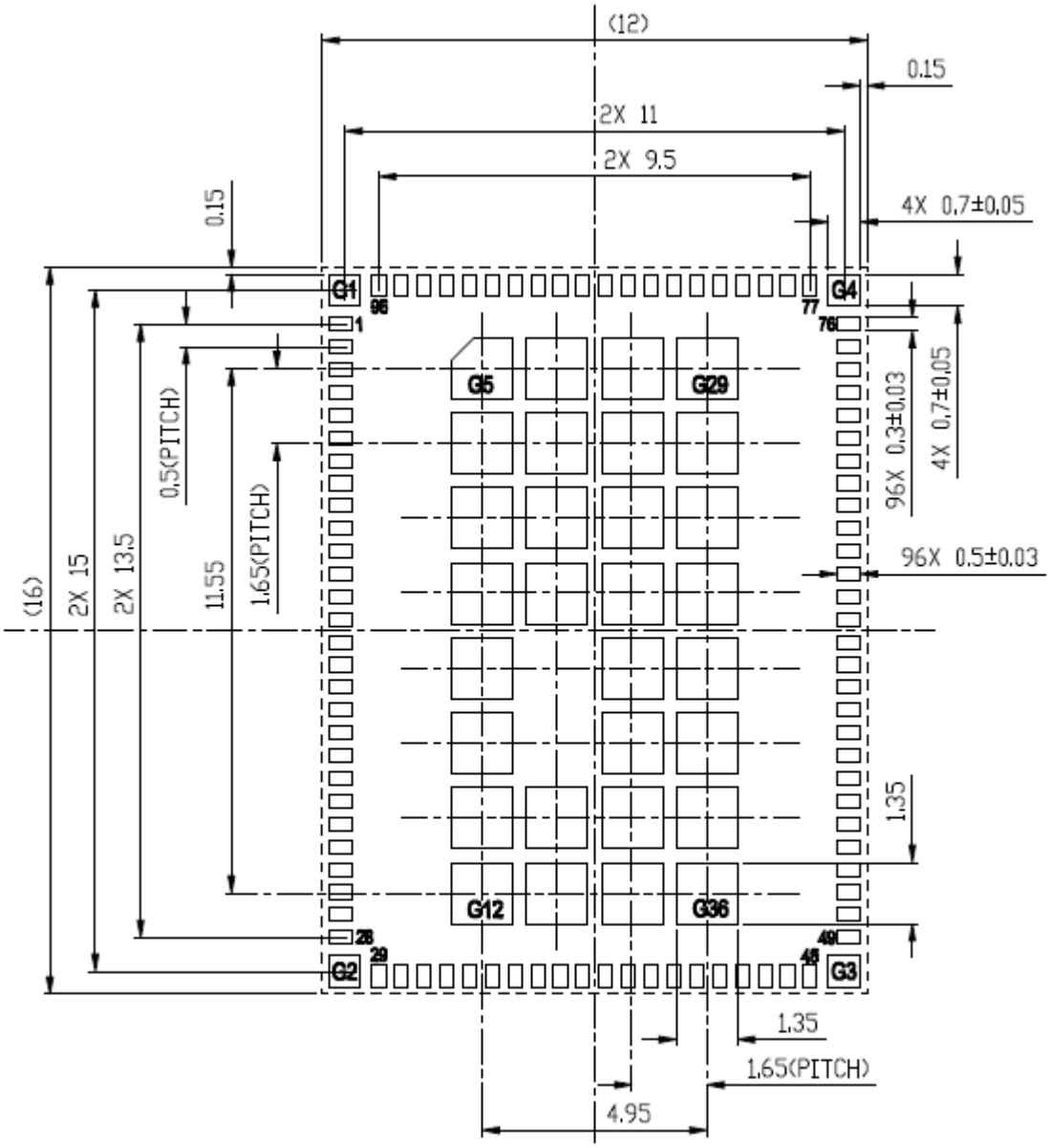
4.2. Pin out drawing



RECOMMENDED SOLDER PAD LAYOUT

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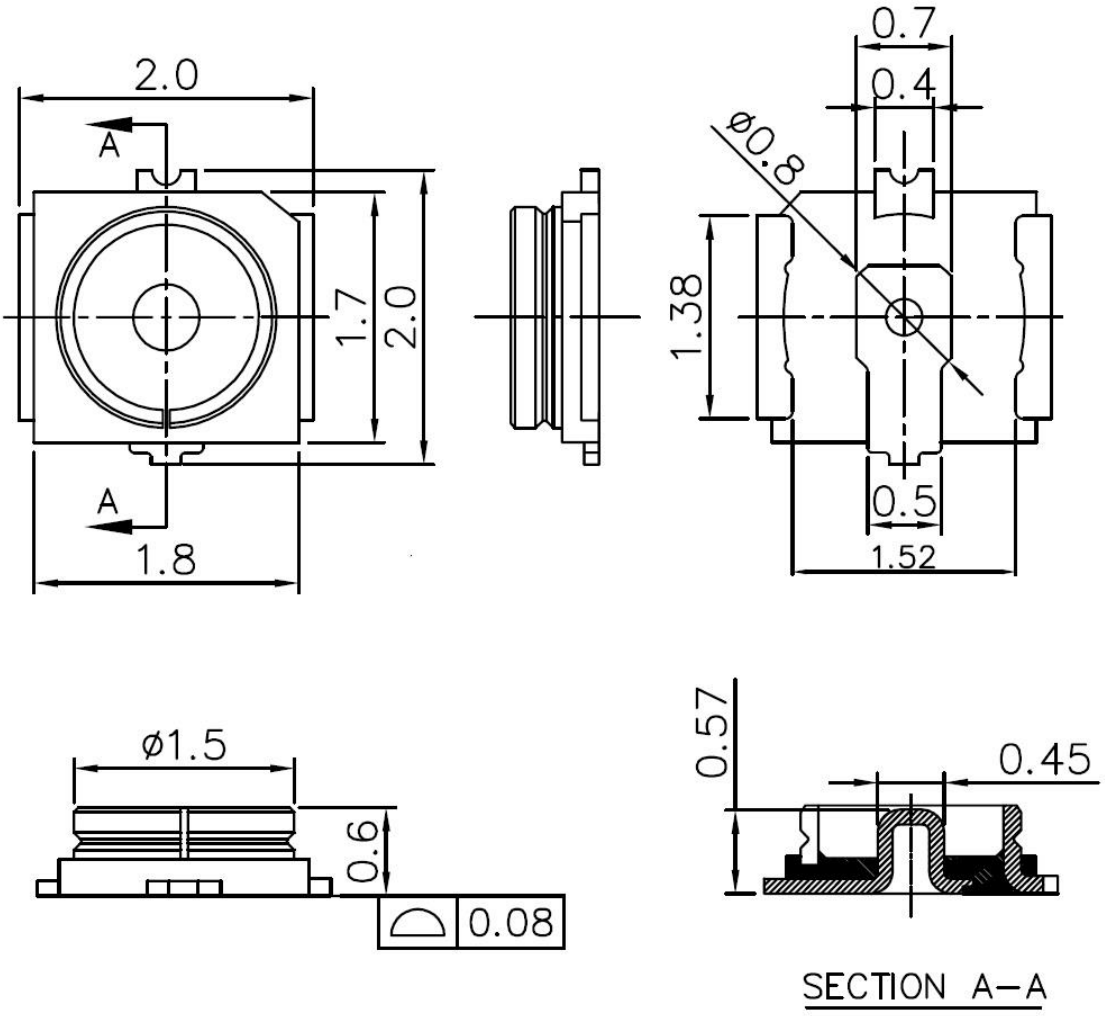
4.3. Antenna connector drawing



UNITS: mm

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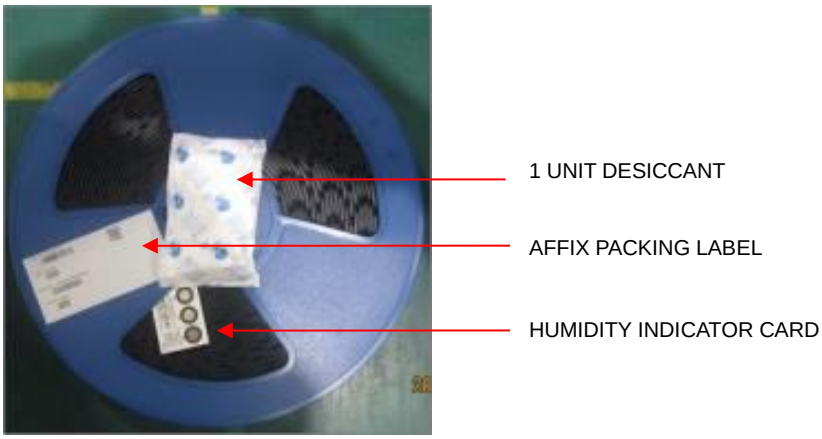
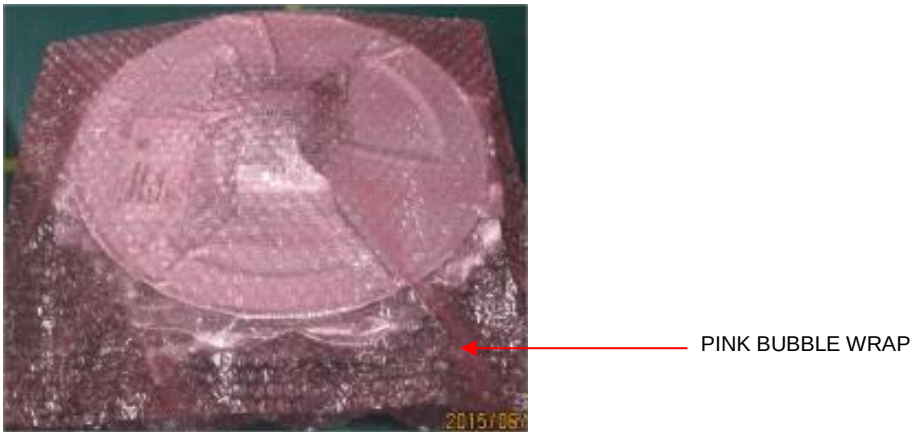
5. Packaging Information

5.1



5.2

5.3



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5.4

5.5

1 Carton= 5 Boxes

5.6

Note: 1 tape reel = 1 box = 1,500pcs

1 carton = 5 boxes = 5 * 1,500pcs=7,500pcs

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